REMARKS

Reconsideration of the subject application is respectfully requested.

In the May 5, 2005 Office Action, all of the pending claims 1-15 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 4,907,148 to Morton ("Morton") in view of U.S. Pat. No. 5,892,729 to Holder, Jr. ("Holder").

Applicants respectfully traverse the Examiner's rejection of claims 1-15.

As to claim 1, the Examiner has indicated that Morton "does not teach gating the row mask signal and column mask signal with a clock signal of each cell to activate, at the next clock cycle, the enabled cells in the array based on the row mask signal and column mask signal." Official Action, page 2, paragraph 4. The Examiner cites Holder as teaching "an array of selectively enabled memory cells similar to the array of selectively activated processor cells of Morton. Holder further teaches gating the address for the cells to be activated with a clock signal for said cell [col. 3, lines 11-29], in order to conserve power [col. 2, lines 5-36]." *Id.*

As understood by Applicants, the passages in Morton (col. 3, lines 20-51) relied upon by the Examiner describe an arrangement intended to enable processors to perform operations selectively, and not to reduce power consumption. As described in the passage following the passages cited by the Examiner: "This operation forces cells to be idle and results in a completely inefficient use of the array whereby a great deal of time is take in the selection process. Another difficulty arises when one attempts to implement a complex sequence of operations . . . ." Morton, at col. 3, lines 52-57. It is respectfully submitted that even the approach taught by Morton (to address the inefficiencies in the configurations described at col. 3, lines 20-51 in Morton) keeps the processors running and consuming power. In particular, with regard to Morton's Fig. 8, col. 9, line 62 through col. 10, line 6, describe that for each processor the mask pattern "is loaded into the processors which test the data and the sign of the data is pushed into the control register." As can be seen from Fig. 4, and col. 7, lines 51-58, for control register 40, the clock signal, CLK, participates in the entering of data into control register 40 from the right or left, and is continuously supplied to status register 34, multi port RAM 30, and other blocks. Thus, even when not selected, a processor continues to run and to consume power.

As understood by Applicants, Holder proposes the use of enable signals, or other signals, to limit the clocking to individual SRAM memory blocks. Holder, at col. 3, lines 21-33. For example, in Holder's Fig. 1, a decoder 106 is used to generate an enable signal that is

applied to pass transmission gates which allow or prevent the clock signal from clocking particular SRAM memory blocks. Holder, at col. 3, lines 45-67. Further, although the Examiner has cited Figs. 5 and 6 and col. 3, lines 21-25 of Holder in support of his assertion that Holder teaches that an array of memory cells may be enabled by decoded row-and-column addressing means as is well known in the art, Applicants respectfully submit that the cited material show only an arrow 104 labeled "address" and a block 106 labeled "address decoder." No "row-and-column addressing" is mentioned.

Applicants respectfully submit that a *prima facie* case for combining Morton with Holder has not been established by the Examiner. In particular, although the Examiner has indicated that conserving power would be a motivation to combine Morton and Holder, it is respectfully submitted that Morton is silent about any intent or desire to conserve power. Thus, there would be no motivation for one skilled in the art considering Morton and its teachings about processor selection, to look to Holder and its teaching of some power savings by passing or blocking clocks to SRAM blocks. In fact, it is respectfully submitted that combining Holder's approach of passing or blocking clocks to the circuitry in Morton, would prevent Morton's processor selection technique from operating. In particular, as discussed above in Morton, col. 9, line 62 through col. 10, line 6, for each processor the mask pattern "is loaded into the processors which test the data and the sign of the data is pushed into the control register." As can be seen from Fig. 4, and col. 7, lines 51-58, for control register 40, the clock signal, CLK, participates in the entering of data into control register 40 from the right or left, and is continuously supplied to status register 34, multi port RAM 30, and other blocks. It is respectfully submitted that if the clock signal is blocked from a processor in Morton, the processor would be unable to load the data, or to test the data, or to push the sign of data to the control registers, or to perform the other operations needed for the processor to determine whether or not it has been selected. For at least these reasons, it is respectfully submitted that one skilled in the art would be dissuaded from combining Morton and Holder, and it would not be obvious to combine Morton and Holder to obtain the combination set forth in claim 1.

The Examiner's rejection of the other independent claims, 5, 6 and 11, is respectfully traversed for reasons similar to those for claim 1. In particular, a *prima facie* case for combining Morton and Holder has not been established. Further, the asserted combination of Morton and Holder would prevent Morton's processor selection technique from operating. One skilled in the art therefore would be dissuaded from combining Morton and Holder, and it would not be

obvious to combine Morton and Holder to obtain the combination set forth in independent claims 5, 6 and 11.

For at least the foregoing reasons it is respectfully submitted that independent claims 1, 5, 6 and 11 are allowable over Morton and Holder. As to dependent claims 2-4, 7-10, and 12-15, it is respectfully submitted that these claims, as ultimately dependent from allowable base claims, are themselves allowable.

The Commissioner is hereby authorized to charge any fees that may be associated with this communication to Deposit Account No. 07-1896.

Respectfully submitted,

DLA PIPER RUDNICK GRAY CARY US LLP

Date: October 31, 2005

By: _____
Gerald T. Sekimura
Reg. No. 30,103

DLA PIPER RUDNICK GRAY CARY US LLP
153 Townsend Street, Suite 800
San Francisco, CA 94107
Telephone: 415-836-2500
Facsimile: 415-836-2501

Customer No. 29585